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JAW

PATENT APPLICATION
Docket No. 1482-177

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Barrie Gilbert

Serial No.: 10/766,514 Examiner: Minh T. Nguyen

Filed: January 27, 2004 Group Art Unit: 2816

For: SQUARING CELLS AND MULTIPLIERS USING SUMMED EXPONENTIALS

Date: November 16, 2005

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

## TRANSMITTAL OF APPEAL BRIEF

This Appeal Brief is in furtherance of the Notice of Appeal mailed in this case on August 16, 2005. Appeal is taken from the Final Office Action mailed May 16, 2005 finally rejecting claims 12, 13, 15, 17, 19, 21, 22 and 24-26.

Also enclosed is:

☒ Form PTO-2038 authorizing payment in the amount of $620.00 for the Appeal Brief fee ($500.00) and one month extension fee ($120.00)

☒ Applicant petitions the Commissioner to extend the time for response. The extension fee is included and a duplicate copy of this form is enclosed.

☒ Any deficiency or overpayment should be charged or credited to deposit account number 13-1703.

**CUSTOMER NO. 20575**

Respectfully submitted,

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The fees required under §1.17(c) and any required petition for extension of time for filing this Brief and fees are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

## REAL PARTY IN INTEREST

The present application has been assigned to the following party:

Analog Devices, Inc.
One Technology Way
Norwood, MA 02062

## RELATED APPEALS AND INTERFERENCES

The Board's decision in the present Appeal will not directly affect, or be directly affected, or have any bearing on any other appeals or interferences known to the appellant, or to the Applicant's legal representative.

## STATUS OF CLAIMS

Claims pending in the application: 12-31

Claims rejected: 12, 13, 15, 17, 19, 21, 22 and 24-26 (which are finally rejected)

Claims appealed: 12, 13, 15, 17, 19, 21, 22 and 24-26

Claims allowed: 28-31

Claims objected to: 14, 16, 18, 20, 23 and 27

## STATUS OF AMENDMENTS

No amendments have been filed subsequent to final rejection.

## SUMMARY OF CLAIMED SUBJECT MATTER

Claim 12 is drawn to a squaring cell formed from two sub-exponential current generators that are coupled together such that their outputs are combined to produce an approximate square-law function. An example embodiment of such a squaring cell is shown in Fig. 20 and described in the specification at page 17, line 19, through page 19, line 26. An embodiment of a sub-exponential current generator is described in the specification at page 19, lines 9-18.

Claim 15 is drawn to a method for squaring a signal by generating and combining first and second sub-exponential currents. This method may be understood in the context of the embodiment of Fig. 20 as discussed above with reference to claim 12.

Claim 17 is drawn to a method for squaring a signal by generating and combining first and second currents that vary exponentially (possibly, but not necessarily, sub-exponentially), and scaling the currents *while* combining them. An embodiment that illustrates this claim is described in the specification at page 20, lines 24-28.

Claim 19 is drawn to a method for squaring a signal by generating first and second exponential currents in response to an input signal, combining the currents, and altering the currents to provide sub-exponential currents. An example embodiment that illustrates this method is described in the specification at page 19, lines 4-8 with reference to Fig. 20.

Claim 21 is drawn to a multiplier that includes four sub-exponential current generators that are coupled together in pairs to create a multiplier. An example embodiment of such a multiplier is shown in Fig. 21 and described in the specification at page 20, line 32, through page 22, line 14. The embodiments of the sub-exponential current generators utilized in the circuit of Fig. 21 are in most respects that same as the sub-exponential current generators

utilized in the circuit of Fig. 20 and described in the specification at page 19, lines 9-18.

Claim 24 is drawn to a method for multiplying two input signals by generating four currents that vary sub-exponentially in response to the input signal, and combining the currents in a specific combination that yields a multiplication function. This method may be understood in the context of the embodiment of Fig. 21 as discussed above with reference to claim 24.

## GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 12-13, 15 and 19 are unpatentable under 35 USC 102(e) as being anticipated by U.S. Patent No. 5,909136 to Kimura ("Kimura").

Whether claims 17, 21-22 and 24-26 are unpatentable under 35 USC 102(e) as anticipated by, or in the alternative, under 35 USC 103(a) as obvious in view of U.S. Patent No. 5,909136 to Kimura ("Kimura").

## ARGUMENT

### Anticipation Rejection under 35 USC 102(e) based on U.S. Patent No. 5,909136 to Kimura

#### Claims 12, 13, 15 and 19

A prior technique for achieving a square-law function involves the use of two opposing exponential current generators that are arranged so that their currents are combined to produce a single output current that obeys an approximate square-law. This is graphically illustrated in Fig. 3 of Kimura which shows how the output $I_{D3}$ from a first exponential current generator and the output $I_{D2}$ from a second exponential current generator may be summed to produce a final output $I_{SQ}$ that approximates a square-law.

Claim 12 recites a squaring cell having two sub-exponential current generators. A sub-exponential current generator differs from a true exponential current generator in that it produces a current having an output function that is deliberately "softened" to result in an output that deviates from an ideal exponential function. (Page 19, lines 12-16.) Purposely softening the exponential functions of the current generators may cause the combined output to more closely approximate an ideal square law. (Page 19, lines 16-18.) In other words, combining two *true* exponential functions produces an inaccurate square-law, but combining two *sub*-exponential functions may produce a more accurate square-law.

An embodiment of squaring cell having sub-exponential current generators is shown in Fig. 20 of the present application. In the absence of the two resistors $R_S$ in Fig. 20, the current generators 52 and 54 would be true exponential current generators due to the exponential characteristic of the transistors as explained in the specification at page 17, line 30 through page 18, line 8. The inclusion of resistors $R_S$, however, alters the outputs $I_{C1}$ and $I_{C2}$ so as to soften the shape of the exponential functions, thereby providing a better approximation of a true square-law as described in the specification at page 19, lines 5-7.

The Examiner argues that Kimura discloses sub-exponential current generators because the exponential function set forth in equation 17 (col. 8, line 18) is based on an approximation. Specifically, the Examiner points to Kimura's assumption, while deriving equation 17, that the DC common-base current gain factor $\alpha_F$ for a transistor is equal to 1, when in practice, $\alpha_F$ is typically equal to 0.98-0.99 for a transistor made with ordinary semiconductor device manufacturing processes. (Col. 8, lines 3-6.)

However, the Examiner has failed to show how, if at all, this approximation affects the exponential relationship. There is no argument or evidence as to whether an $\alpha_F$ that is not unity (not equal to one) would soften the exponential function (which *would* create a sub-exponential function), sharpen the exponential function (which would create something that might be deemed a super-exponential function rather than sub-exponential), have some other effect, or have no effect at all.

In essence, the Examiner is arguing that Kimura inherently discloses a sub-exponential current generator. But in relying upon a theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic <u>necessarily</u> flows from the teachings of the prior art. MPEP 2112. Since the Examiner has not shown how a sub-exponential current generator necessarily flows from the teachings of Kimura, the rejection of claim 12 is not properly supported. Similar reasoning applies to the rejection of claims 13, 15 and 19.

<u>Obviousness Rejection under 35 USC 103(a) based on U.S. Patent No. 5,909136 to Kimura</u>

<u>Claims 17 and 26</u>

Claim 17 recites scaling the first and second currents responsive to a control signal *while* generating and combining the first and second currents. In other words, the scaling is performed while the circuit is in operation. In the embodiment of Fig. 20, scaling may be

accomplished by varying the bias currents $I_0$ in response to a control signal as explained in the specification at page 20, lines 24-27. The specification discloses at page 20, line 28 that scaling the first and second currents while the circuit is in operation may provide the benefit of allowing squaring and weighting functions to be performed simultaneously.

Kimura discloses varying certain bias signals by programming them in a manner that would have the effect of scaling the first and second currents. (Col. 8, lines 57-58.) However, the Examiner acknowledges that Kimura does not disclose programming the bias signals while the circuit is in operation. Kimura only mentions that programming the bias signals allows for easy circuit design and integration in large scale integration (LSI). (Col. 8, lines 58-62.) From this, the Examiner makes the analytical leap that it would have been obvious to perform the scaling operation while the circuit is in operation because it would be desirable to do so because the circuit does not need to be powered down.

This is an impermissible hindsight reconstruction using the Applicant's disclosure as a roadmap to achieve the claimed invention. It is axiomatic that, when the cited reference does not disclose a claimed feature, there must be some motivation or suggestion *in the art* to modify the reference to achieve the claimed invention. The Examiner has not identified any motivation or suggestion in Kimura, or any other reference, to scale the currents while the circuit is in operation. The Examiner's conclusory allegation that it would have been understood by a person of ordinary skill in the art to be desirable to do so is inadequate to establish such motivation or suggestion. Thus, a prima facie case of obviousness has not been established for claim 17. Similar reasoning applies to the rejection of claim 26.

<u>Claims 21 and 24</u>

For purposes of this appeal, claims 21 and 24 stand or fall with claims 12, 13, 15 and 19. Claim 21 recites four sub-exponential current generators. Claim 24 recites generating four currents that vary sub-exponentially. In explaining the rejection of claims 21 and 24, the Examiner consistently refers to exponential rather than sub-exponential current generators (except for one instance). As argued above, Kimura does not disclose sub-exponential currents or current generators, and the Examiner has not set forth any argument that they would have been obvious in view of the prior art.

Claims 22 and 25

For purposes of this appeal, claims 22 and 25 stand or fall with claims 12, 13, 15 and 19.

## CONCLUSION

Applicant requests that the rejection of claims 12, 13, 15, 17, 19, 21, 22 and 24-26 be reversed.

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Respectfully submitted,

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## CLAIMS APPENDIX

12. (Rejected) A squaring cell comprising:

a first sub-exponential current generator for generating a first current responsive to an input signal; and

a second sub-exponential current generator for generating a second current responsive to the input signal;

wherein the first and second exponential current generators are coupled together to combine the first and second currents.

13. (Rejected) A squaring cell according to claim 12 wherein each of the sub-exponential current generators includes:

a constant current stack coupled to a first input terminal; and

a variable current stack coupled to a second input terminal and the constant current stack.

15. (Rejected) A method for squaring a signal comprising:

generating a first current which varies sub-exponentially responsive to the signal such that the first current increases when the signal increases;

generating a second current which varies sub-exponentially responsive to the signal such that the second current decreases when the signal increases; and

combining the first and second currents.

17. (Rejected) A method for squaring a signal comprising:

generating a first current which varies exponentially responsive to the signal such that the first current increases when the signal increases;

generating a second current which varies exponentially responsive to the signal such that the second current decreases when the signal increases;

combining the first and second currents; and

scaling the first and second currents responsive to a control signal while generating and combining the first and second currents.

19. (Rejected) A method for squaring a signal comprising:

generating a first current which varies exponentially responsive to the signal such that the first current increases when the signal increases;

generating a second current which varies exponentially responsive to the signal such that the second current decreases when the signal increases;

combining the first and second currents; and

altering the first and second currents so as to provide sub-exponential functions.

21. (Rejected) A multiplier comprising:

a first sub-exponential current generator for generating a first current responsive to a first input signal and a second input signal;

a second sub-exponential current generator for generating a second current responsive to a third input signal and a fourth input signal;

a third sub-exponential current generator for generating a third current responsive to the first input signal and the fourth input signal; and

a fourth sub-exponential current generator for generating a fourth current responsive to the third input signal and the second input signal;

wherein the first and second sub-exponential current generators are coupled together to combine the first and second currents; and

wherein the third and fourth sub-exponential current generators are coupled together to combine the third and fourth currents.

22. (Rejected) A multiplier according to claim 21 wherein each of the sub-exponential current generators includes:

a constant current stack coupled to a first input terminal; and

a variable current stack coupled to a second input terminal and the constant current stack.

24. (Rejected) A method for multiplying a first signal and a second signal, wherein the first input signal is the difference between a first signal and a third signal, and the second input signal is the difference between a second signal and a fourth signal, the method comprising:

generating a first current which varies sub-exponentially responsive to the first signal and the second signal;

generating a second current which varies sub-exponentially responsive to the third signal and the fourth signal;

generating a third current which varies sub-exponentially responsive to the fourth signal and the first signal;

generating a fourth current which varies sub-exponentially responsive to the second signal and the third signal;

combining the first and second currents; and

combining the third and fourth currents.

25. (Rejected) A method according to claim 24 wherein:

combining the first and second currents includes summing the first and second currents; and

combining the third and fourth currents includes summing the third and fourth currents.

26. (Rejected) A method according to claim 24 further including scaling the first, second, third, and fourth currents responsive to a control signal while generating and combining the currents.

EVIDENCE APPENDIX

None.

## RELATED PROCEDINGS APPENDIX

None.